

12.7 A 3.125Gb/s Limit Amplifier with 42dB Gain and 1 μ s Offset Compensation in 0.18 μ m CMOS

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High-gain amplifiers require offset compensation (OC) to achieve high input sensitivity. The classical way to achieve such compensation in wide bandwidth applications with NRZ data streams, as encountered in SONET applications, is to feed the output of the amplifier back to its input through a low bandwidth filter [1,2], such as an RC filter, as shown on the left side of Fig. 12.7.1. Unfortunately, this approach leads to an undesirable tradeoff between OC settling time and output jitter – a higher OC bandwidth has the benefit of achieving faster settling time at the expense of higher data dependent jitter. As a result of this limitation, current approaches suffer from long compensation times (typically >1ms for SONET OC48 applications) and often require an off-chip capacitor to achieve acceptably low compensation bandwidths. Although the long compensation times are acceptable for point-to-point links, they pose a severe obstacle for upcoming many-to-one links since each input channel may have different power levels and therefore demand different offset settings for the amplifier. The speed of the OC loop will therefore determine how quickly one can switch between channels.

We propose a compensation scheme that uses a new CMOS peak detector (PD) structure and a variable-tap feedback system to dramatically improve the tradeoff between OC settling time and data-dependent jitter due to the offset correction loop. We will show that the approach enables settling times on the order of 1 μ s while simultaneously achieving jitter that meets SONET OC48 specifications. Thus, the proposed system enables an improvement of over 3 orders of magnitude in OC time over the classical approach, while still maintaining very low data-dependent jitter levels.

The key principle of our technique is to use the fact that the offset of a differential amplifier can be estimated from the difference in the *peak* values of its two outputs as shown in Fig. 12.7.2 (note that we assume equal gains through each of the data paths, which is reasonable for integrated amplifier designs). Therefore, the proposed OC technique, shown on the right side of Fig. 12.7.1, replaces the LPF in the offset feedback path with a PD and integrator. The PD measures the output-referred offset of the limit amplifier (LA), and the integrator filters the instantaneous PD output and forces the steady-state, output-referred offset voltage to be zero regardless of the loop gain. Since peak information is lost when an amplifier stage becomes saturated, PDs are placed at the outputs of each LA stage and the last unsaturated output is used to sense the offset, as shown in Fig. 12.7.3. The same PDs, along with digital selection logic, are used to determine which stage has the last unsaturated output. Since the PDs are small and consume little power, multiple inclusions of them do not pose a significant power or area penalty.

While the use of peak detection for offset cancellation is not a new concept [3], its implementation in pure CMOS has previously proven challenging due to the lack of good diode structures. While CMOS transistors can be used to perform diode functions (i.e. as source followers), as shown at the left of Fig. 12.7.4, the resulting circuit has very limited high frequency capability. In particular, source followers require a considerable amount of channel current to achieve fast settling time, but the presence of such current leads to severe droop problems. Therefore, the clas-

sical use of CMOS source followers as PDs presents an unacceptable tradeoff between settling time and droop.

To dramatically improve the tradeoff between settling time and droop, we propose the CMOS PD structure shown at the right of Fig. 12.7.4. The key to its operation is the assumption that the amplifier is differential and that it is processing NRZ data, so that the PD implementation is also differential and has an input signal that primarily alternates between two different voltage levels. As such, we can use the input signal to switch the PD bias current between the two source follower circuits of the differential PD. The inclusion of the current switching dramatically alters the settling time and droop tradeoff – it allows a relatively high bias current to run through the source follower circuit when it is following the peak of the input signal, but eliminates the droop problems of this higher current by removing the current bias when the source follower circuit is trying to hold the peak value. Due to incomplete switching of the current pair with a practical switch circuit implemented as a differential pair (Fig. 12.7.4), there is still some amount of droop in the PD. However, the improvement of the settling time and droop tradeoff is dramatic compared to the classical source follower approach, and thereby allows a dramatic improvement in settling times.

To demonstrate the technique, a 7-stage resistively-loaded LA, which utilized the proposed OC approach, was fabricated in National Semiconductor's 0.18 μ m CMOS process. The total active area is 0.5mm². The LA stages were designed following the simple numerical design procedure that was developed to allow straightforward design of high-speed, resistively-loaded, differential amplifiers in modern CMOS processes presented in [4]. The design procedure is implemented in a MATLAB script available at www-mtl.mit.edu/research/perrottgrouptools.html. The die was wire bonded in a standard ceramic package, which was then soldered to an FR4 PC board containing low-noise supply voltages and digital interface circuitry. The prototype was tested up to 3.125GHz with a 2³¹-1 PRBS input pattern that had input amplitudes ranging from 2.5mV to 50mV_{pp}. The total differential gain was measured to be 42dB and the power dissipation of the chip is 113mW, excluding the output buffer. Eye diagrams for several input amplitudes at 3.125GHz and a summary of RMS jitter versus input amplitude and data rate are shown in Fig. 12.7.5. Plots of the control voltage step response with a 5mV_{pp} input at 3.125GHz for loop bandwidths of 1, 3 and 5MHz are shown in Fig. 12.7.6. These results demonstrate offset settling times less than 1 μ s while still maintaining SONET OC48 jitter levels. The die photograph is shown in Figure 12.7.7.

Acknowledgements:

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References:

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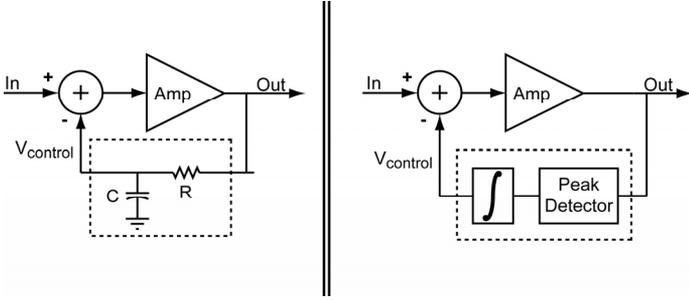


Figure 12.7.1: Traditional and Proposed Offset Compensation.

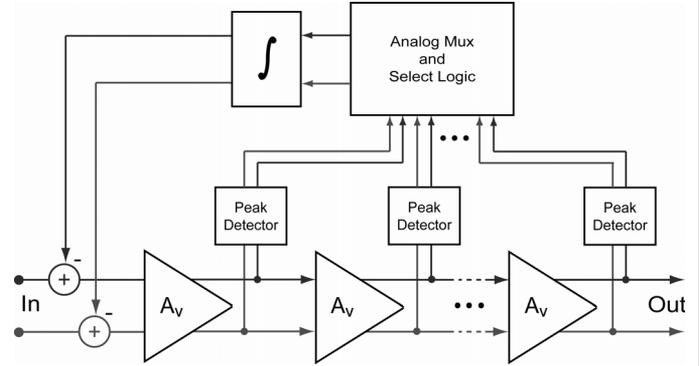


Figure 12.7.2: Dynamic Multi-Tap Offset Compensation.

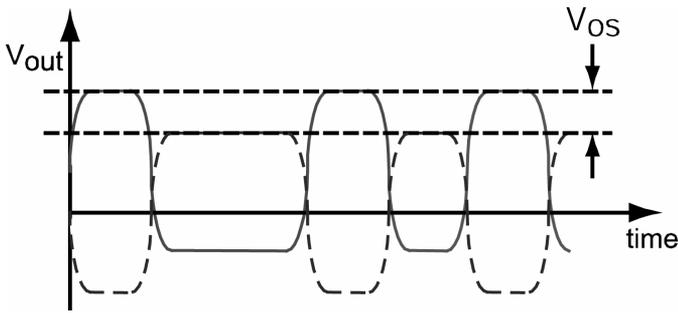


Figure 12.7.3: Offset voltage is estimated by the difference in the peak values of the differential outputs.

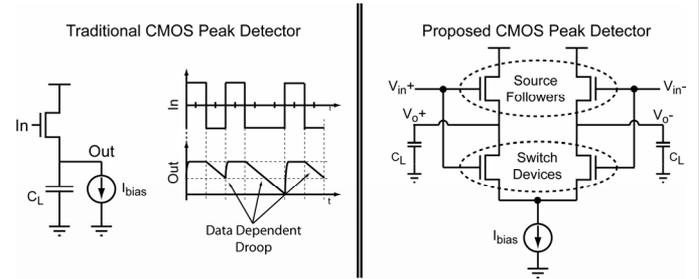


Figure 12.7.4: Traditional and Proposed CMOS Peak Detectors.

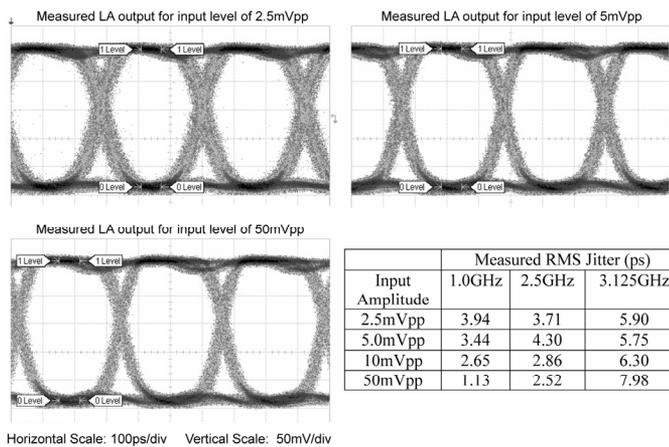


Figure 12.7.5: Measured Eye Diagrams for Various Input Amplitudes.

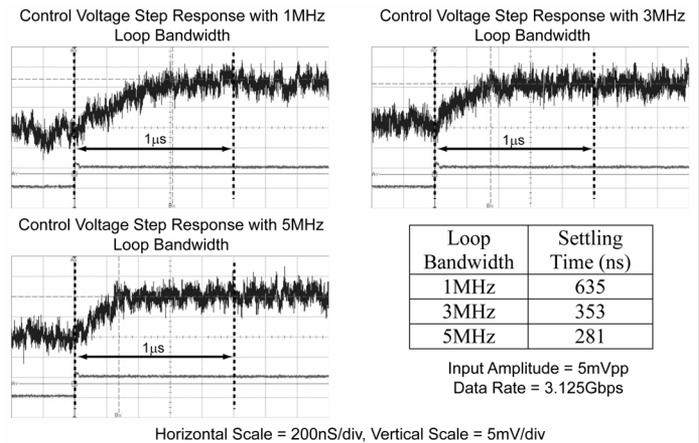


Figure 12.7.6: Measured Step Response vs. Loop Bandwidth.

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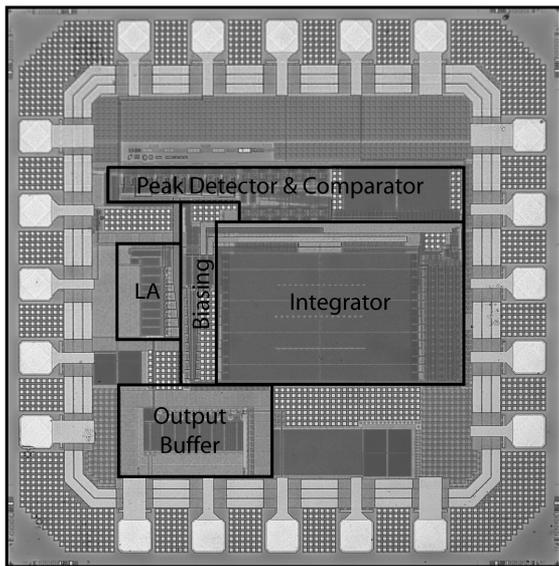


Figure 12.7.7: Die micrograph highlighting major system blocks.