

A 12-Bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer

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Abstract—The use of VCO-based quantization within continuous-time (CT) $\Sigma\Delta$ analog-to-digital converter (ADC) structures is explored, with a custom prototype in 0.13 μm CMOS showing measured performance of 86/72 dB SNR/SNDR with 10 MHz bandwidth while consuming 40 mW from a 1.2 V supply and occupying an active area of 640 $\mu\text{m} \times 660 \mu\text{m}$. A key element of the ADC structure is a 5-bit VCO-based quantizer clocked at 950 MHz which achieves first-order noise shaping of its quantization noise. The quantizer structure allows the second-order CT $\Sigma\Delta$ ADC topology to achieve third-order noise shaping, and direct connection of the VCO-based quantizer to the internal DACs of the ADC provides *intrinsic* dynamic element matching of the DAC elements.

Index Terms—Analog-to-digital conversion, quantizer, ring oscillator, sigma-delta, voltage-controlled oscillator (VCO), VCO-based.

I. INTRODUCTION

IN THIS PAPER, we explore the use of a multi-phase voltage-controlled oscillator (VCO) for quantization within a continuous-time (CT) $\Sigma\Delta$ analog-to-digital converter (ADC) structure. Our goals are to summarize previous theoretical work in this area, explore the various circuit issues that must be addressed to achieve high performance, and demonstrate the approach with measured results from a physical prototype. The presented ADC architecture, which operates at a clock rate of 950 MHz, achieves an SNR/SNDR of 86/72 dB in 10 MHz of input bandwidth while consuming 40 mW from a 1.2 V supply in 0.13 μm CMOS [1].

We begin by providing background of VCO-based quantizers, pointing out their first-order noise-shaping properties, and discussing the merits of a particular circuit topology for achieving high-speed clock rates. In Section III, we then explore limitations in achieving high SNDR in this structure by modeling its key nonidealities, the chief of which is nonlinearity in the VCO voltage-to-frequency tuning curve. Section IV points out that the impact of this nonlinearity is mitigated by placement of the VCO-based quantizer within a CT $\Sigma\Delta$ ADC structure and discusses a means of achieving *intrinsic* dynamic element matching (DEM) of the DAC elements used within the $\Sigma\Delta$ ADC through proper connection with the VCO-based quantizer. Finally, Section V presents the proposed ADC and its accompanying circuits, Section VI provides measured results of the prototype, and Section VII concludes.

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II. BACKGROUND

Here, we first cover basic concepts related to VCO-based quantization and then present a preferred circuit topology for achieving high-speed sampling and low latency as required for quantizers placed within CT $\Sigma\Delta$ ADC structures.

A. Basic Concepts

Fig. 1 illustrates a conceptual view of using a VCO, which corresponds to a multi-phase ring oscillator, to achieve quantization of an input analog voltage. The key idea is to count the number of oscillator edges that occur within each period of an input clock signal. The count values, which are digital in nature, provide a quantized estimate of the input analog voltage on V_{tune} according to the mapping between the tuning voltage and output frequency of the VCO. The resolution of the VCO-based quantizer is a function of the ratio of the clock period to the time spacing of the oscillator edges, which leads to a tradeoff between sample rate and the number of quantizer levels for these structures.

As revealed by Fig. 1, VCO-based quantization carries the very attractive aspect of having a highly digital implementation. Also, these structures strongly take advantage of Moore's law since their resolution versus sampling speed tradeoff relationship directly improves with the reduced gate delays of modern CMOS processes. As such, there has been an increasing level of interest in using VCO-based quantization to achieve analog-to-digital (A/D) conversion in modern mixed-signal circuits [2]–[6].

One very interesting aspect of VCO-based quantizers is their potential ability to achieve first-order noise shaping of their quantization noise [7]. Fig. 2 illustrates this principle in simplified form by examining the counting process of one phase of the oscillator with a constant V_{tune} input. The key point here is that the truncation error $q[k]$ at the end of a clock period boundary is not lost, but rather it is accounted for in the following measurement. Therefore, we find that the overall quantization error signal can be described by $\text{Error}[k] = q[k] - q[k-1]$, which reveals first-order noise shaping, under the assumption that $q[k]$ has a white noise profile.

B. High-Speed Sampling Implementation

While the VCO-based quantizer shown in Fig. 1 provides a convenient illustration of the basic principles involved, its practical implementation is problematic due to the reset operation that is used on its counters. Indeed, in cases where a VCO edge occurs in close proximity to the reset signal (which will occur

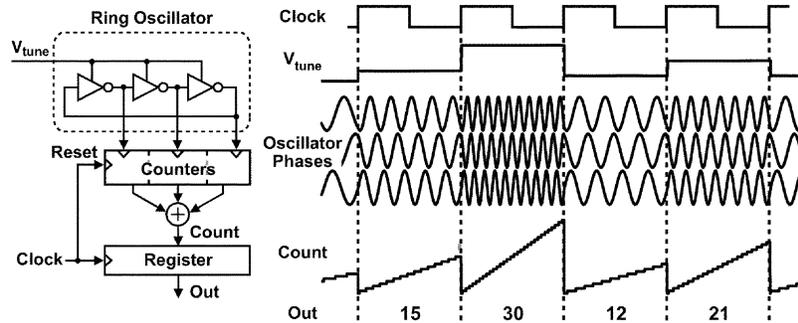


Fig. 1. VCO-based quantizer leveraging a multi-phase oscillator.

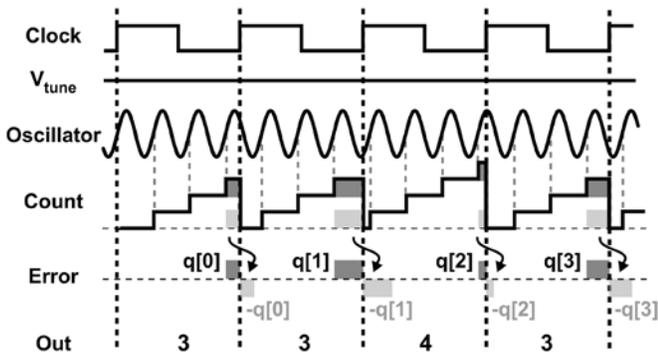


Fig. 2. Illustration of first-order noise-shaping property of VCO-based quantizers.

quite often), the measured edge count is likely to become corrupted due to the propagation delay characteristics of the counters and the need for adequate setup times on the sampling registers. This count corruption process will, in turn, destroy the desired noise shaping properties of the structure.

There are a variety of alternative VCO-based quantizer structures that could remove the reset issue just discussed; we will focus here on one suited for high sample rate operation as shown in Fig. 3 [6]. In this structure, the multi-bit counters and resettable registers shown in Fig. 1 are avoided in favor of a simpler implementation that simply requires a set of standard registers (with no reset), XOR gates, and a final adder stage. We see that an explicit reset operation is avoided, and the relative simplicity of this circuit allows high speed operation with small latency, which are important characteristics when placing the VCO-based quantizer within a CT $\Sigma\Delta$ ADC structure as discussed later in this paper. Note that in this structure, the proposed quantizer expands the number of delay elements such that the number of transitions per clock period is smaller than that number of elements.

The binary sequences shown in Fig. 3 are useful for understanding the operation of the high speed quantizer structure. The key idea is to observe whether a given VCO delay cell undergoes a transition within a given clock period by comparing samples of its current and previous states with an XOR operation. The number of VCO delay cells that undergo a transition within a given clock period is a function of the delay through each stage as set by the V_{tune} voltage, which yields the quantized value of the V_{tune} voltage that we seek. An important observation from

Fig. 3 is that the XOR outputs barrel-shift through their values with each progressing sample. This property will be exploited later in this paper.

III. SNDR LIMITATIONS FOR VCO-BASED QUANTIZATION

To better understand the properties of VCO-based quantizers, Fig. 4 depicts a functional block diagram of the VCO-based quantizer and its corresponding linearized frequency domain model. Comparing the block diagram with the corresponding quantizer structure in Fig. 3, the VCO block corresponds to the ring oscillator, and the Quantizer block corresponds to the first set of registers which sample the quantized phase signal of the VCO. The First Order Difference block corresponds to comparison of the register values to their previous sample values by the XOR gates in Fig. 3. In the corresponding frequency-domain model, the VCO is represented as an integrator with gain $2\pi K_v$, which represents conversion of the V_{tune} voltage to a VCO phase signal, and the addition of phase noise. The Quantizer is modeled as a sampler that adds quantization noise, and the First Order Difference block is seen as a $1 - z^{-1}$ transfer function that approximates a differentiation operation, and thereby converts the VCO phase signal to a corresponding VCO frequency signal.

A key observation offered by Fig. 4 is that the quantization noise is first-order noise-shaped by virtue of the first-order difference operation shown in the figure, which is in agreement with the time-domain view of the quantization noise from Fig. 2. We also see that the VCO phase noise is shaped as well, but the result of such shaping is a flat spectrum due to the -20 dB/dec slope of the original phase-noise signal. In reality, the shaped VCO phase noise will also include $1/f$ noise, but this is ignored here for the sake of modeling simplicity.

An important issue that was neglected in Fig. 4 is that the voltage-to-frequency tuning curve of a VCO is quite nonlinear in practice. Fig. 5 shows that the impact of such nonlinearity is to introduce harmonic distortion which can significantly degrade the SNDR performance of the quantizer. For example, a typical VCO with 5% tuning nonlinearity will have an SNDR limited to 6 bits, and additional effort to improve this has been limited to 8-bit performance [5]. Therefore, VCO nonlinearity forms the primary bottleneck to achieving high SNDR values for the VCO-based quantizer. It is this issue that leads us to the $\Sigma\Delta$ ADC architecture presented in Section IV.

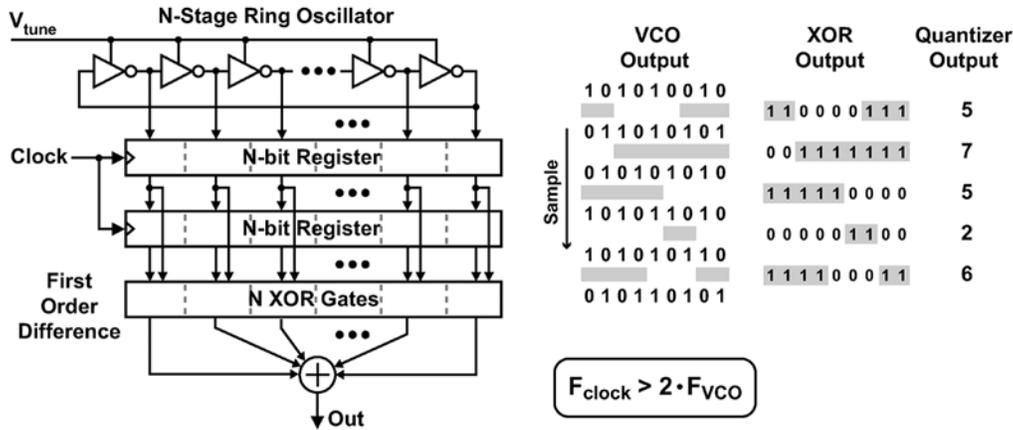


Fig. 3. High-speed multi-phase VCO frequency measurement.

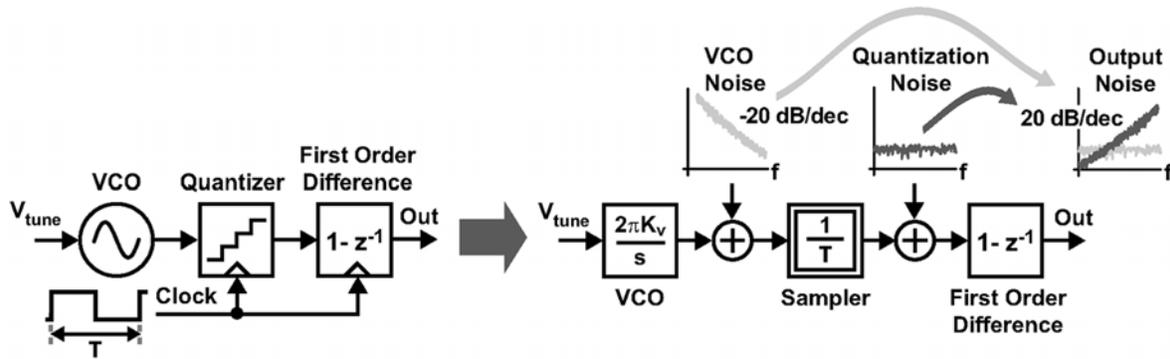


Fig. 4. Block diagram model and corresponding linearized frequency-domain model of the VCO-based quantizer.

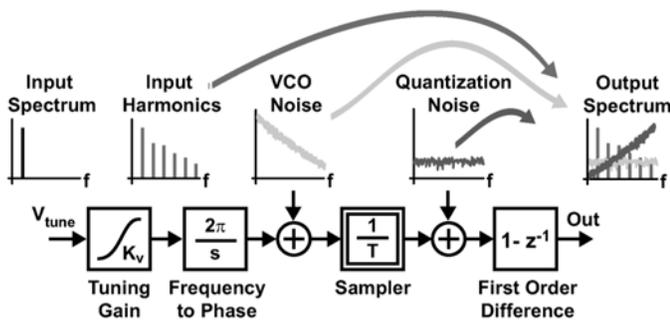


Fig. 5. Behavioral model illustrating the VCO quantizer nonlinearity.

IV. LINEARIZATION OF VCO-BASED QUANTIZERS USING FEEDBACK

Fig. 6 displays the use of feedback to improve the linearity performance of the VCO-based quantizer, which corresponds to a CT $\Sigma\Delta$ ADC with a multi-bit quantizer [2], [6]. As illustrated by the figure, the presence of high gain before the quantizer suppresses the nonlinearity of the quantizer by allowing the feedback to appropriately pre-distort the input to the quantizer. In addition, the high gain also reduces the impact of both quantization noise and VCO phase noise on the overall ADC performance by lowering their influence on the input-referred noise of the ADC.

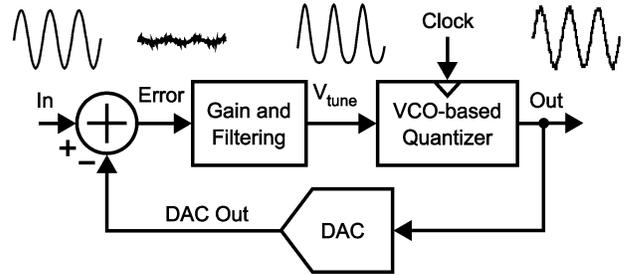


Fig. 6. $\Sigma\Delta$ feedback to suppress VCO linearity and quantization errors.

A unique attribute of using the VCO-based quantizer within a $\Sigma\Delta$ ADC structure is that the overall quantization noise shaping is the *sum* of the first-order shaping from the VCO-based quantizer and the order of the loop dynamics. This implies that the designer is able to gain an additional order of noise shaping with the VCO-based quantizer without significantly impacting loop dynamics. As an example, a classical second-order $\Sigma\Delta$ design, which is well known for its robust stability characteristics, can achieve a much more desirable third-order noise-shaping characteristic. In the case of seeking more aggressive noise shaping with higher order structures, the issue of controlling VCO quantizer gain and dealing with any additional latency must be carefully considered.

The VCO-based quantizer structure shown in Fig. 3 adds another significant benefit within the $\Sigma\Delta$ ADC structure due to

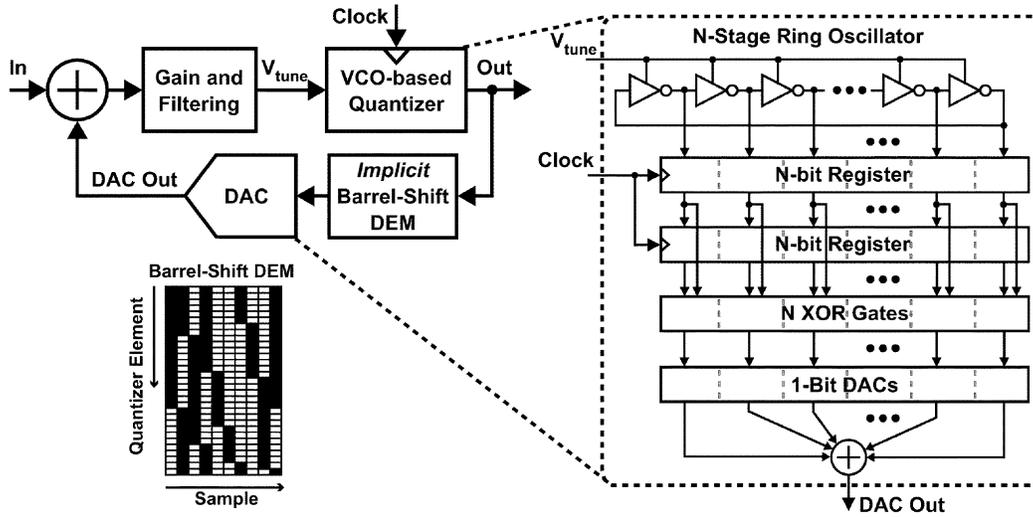


Fig. 7. Utilizing VCO for implicit barrel shift DEM of DAC elements.

the barrel shifting characteristic of its XOR gate outputs. As shown in Fig. 7, direct connection of the XOR outputs of the quantizer to the thermometer-coded inputs of the DAC within the $\Sigma\Delta$ feedback loop provides *implicit* DEM of the DAC elements [6]. The DEM operation acts to noise shape the impact of mismatch between the DAC elements, which is important so that mismatch does not become the bottleneck to achieving high resolution in the overall ADC. The implicit DEM implementation offered by the VCO-based quantizer carries no penalty in terms of latency or power and is therefore a very attractive feature of this structure.

Lastly, it is worthwhile to consider a useful advantage of the VCO-based quantizer over classical comparator-based, multi-level quantizers with respect to metastability behavior. In the case of the VCO-based quantizer, all of its phase taps will be at ground or supply voltage at any given time *except* for the one phase tap that is undergoing transition (from ground to supply or vice versa). Therefore, movement between two levels of the VCO-based quantizer involves a voltage transition of magnitude equal to the supply voltage (i.e., V_{DD}). In contrast, movement between two levels of a comparator-based topology involves a voltage transition with maximum magnitude equal to V_{DD}/N , where N is the number of quantizer levels. Therefore, the probability of having a metastable event occur with a VCO-based quantizer should be considerably less than that of its comparator-based counterpart due to the fact that its quantization step size is essentially N times larger in voltage. Of course, amplifiers are often included before the comparator-based quantizer to increase its effective quantization step size, but the penalty of doing so is increased power and area.

V. PROPOSED CONTINUOUS-TIME $\Sigma\Delta$ ADC TOPOLOGY

Fig. 8 displays our proposed ADC structure. This circuit topology incorporates an active loop filter, two 31-element current DACs, and a 31-level VCO-based quantizer to achieve *third-order* noise shaping. One should immediately notice the simplicity offered by this structure—the active analog components consist of just one opamp, two current DACs, and

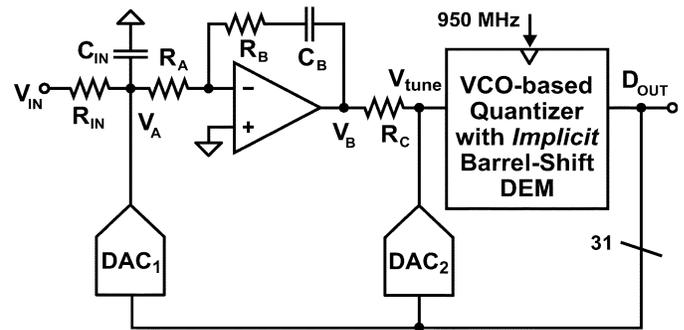


Fig. 8. Block diagram of the proposed ADC.

a ring oscillator (within the VCO-based quantizer). Indeed, the simplicity allows high-speed operation of 950 MS/s to be achieved with compact area and low power dissipation, as will be demonstrated in Section VI. Note that, while a single-ended schematic is shown for clarity, the ADC is fully differential with the exception of a pseudodifferential VCO-based quantizer, as will soon be discussed in more detail.

While the topology shown in Fig. 8 bears resemblance to the popular second-order Candy structure [8], its design is actually quite different with respect to the means by which it achieves stability. In particular, the minor loop feedback, which is created by feeding the output current of DAC₂ into the V_{tune} node, is not formed around an integrator as would be done in the Candy structure. Rather, the two integrators occur before the minor loop and consist of an active integrator (formed by the opamp and elements R_A and C_B) and a lossy integrator (formed passively by elements R_{IN} , C_{IN} , and R_A). Stability of the structure therefore requires the inclusion of an open-loop zero, which is formed by elements R_B and C_B . The function of the minor feedback loop is to compensate for the impact of excess loop delay incurred by the latency of the VCO-based quantizer [9]. With the ADC having a target signal bandwidth of 10–20 MHz, the actual closed-loop bandwidth of the ADC was designed to be around 160 MHz. To achieve adequate phase margin, the stabilizing zero formed by R_B and C_B was set to be in the range of

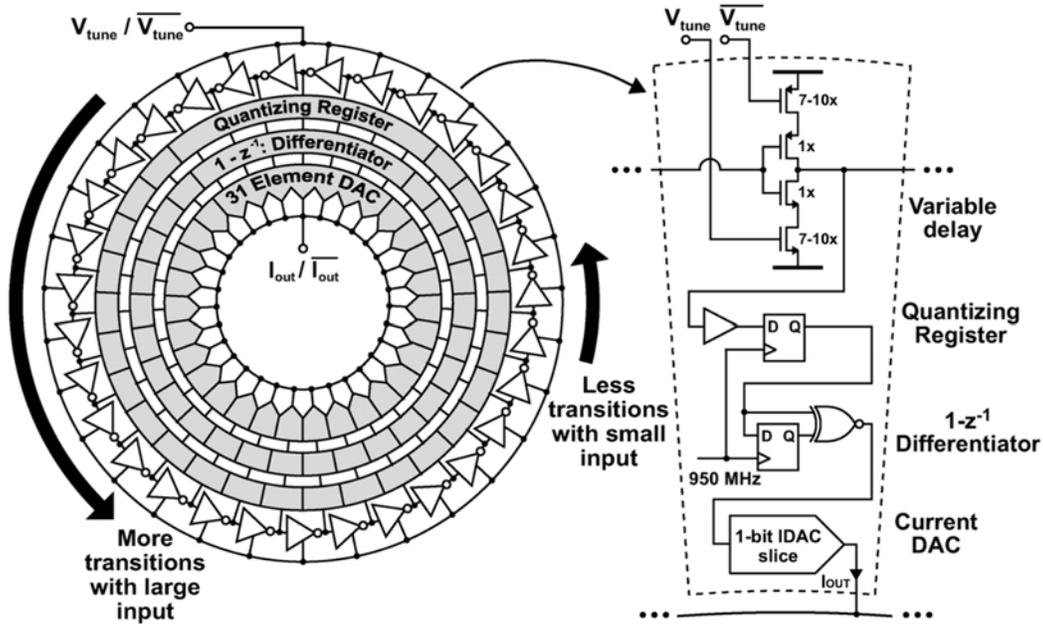


Fig. 9. Geometric view of the proposed 31-level combined VCO quantizer/DEM and DAC.

75–110 MHz (as influenced by the setting of C_B , as explained in the Loop Filter subsection). The passive filter, which forms a lossy integrator as mentioned above, was set to be slightly less than 10 MHz in order to attenuate the large current pulses from the DAC₁ output. While the inclusion of the front-end passive filter leads to a slight penalty in noise, it has the advantage of providing a very linear front-end for the ADC and simplifying design of the opamp (which would otherwise have to deal more directly with the current pulses of DAC₁).

As opposed to optimizing the zeros of the ADC noise transfer function (NTF) for a signal bandwidth of 10–20 MHz, we chose to implement a simple ADC topology that highlights the properties of the VCO-based quantizer. To explain, the proposed topology achieves third-order noise shaping through the inclusion of three zeros within its NTF. Two of those zeros, as provided by the VCO-quantizer and the active integrator, are located at or very near the origin. The third zero, as provided by the lossy integrator formed by the front-end passive filter, is located slightly below 10 MHz as set by the bandwidth of that filter.

While the choice of 10–20 MHz signal bandwidth did not explicitly influence the zero placement, it was strongly considered in choosing appropriate thermal noise levels for the opamp, DAC₁, and the front-end passive filter. These blocks were therefore designed such that the overall thermal noise had a comparable spectral density to the quantization noise at the edge of the signal bandwidth range (i.e., 20 MHz).

Given the above overview of the proposed structure, we now examine its various blocks in detail in the subsections to follow. In particular, we will present additional circuit details of the VCO-based quantizer, the current DACs, and the loop filter.

A. VCO-Based Quantizer

Fig. 9 illustrates a geometric view of the combined VCO-based quantizer, implicit DEM, and DAC circuitry

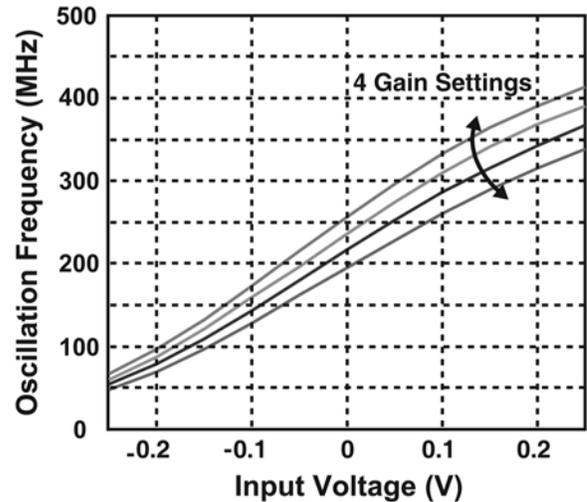


Fig. 10. Tuning characteristic for the proposed VCO-quantizer.

implemented with 31 levels. In essence, this structure corresponds to the VCO-based quantizer shown in Fig. 3, which has been augmented with DAC elements. A bit-slice of this structure, which is also shown in the figure, reveals a variable delay consisting of a four-transistor stack followed by a buffer, some digital logic to implement the first-order difference operation, and a DAC element with current output. The buffer is used to isolate the variable delay output from the sampling register, which is implemented with standard cell regenerative latches. Simulations demonstrated that metastability is not a concern, which offers support to the previous analysis in Section IV. In terms of delay timing, a half-period is available before generating the DAC pulses, which allows use of standard cell XOR gates and TSPC DFF for the subsequent first-order difference logic.

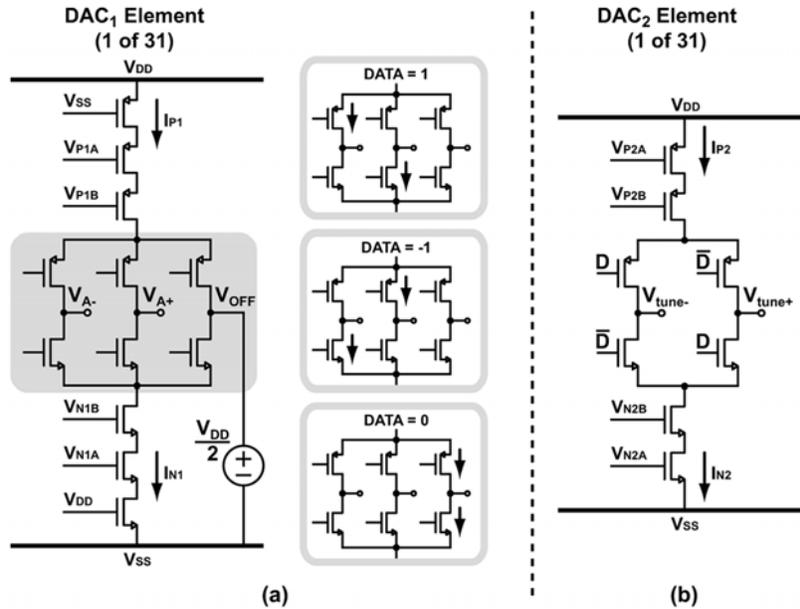


Fig. 11. Schematic and operation of (a) DAC_1 and (b) DAC_2 .

There are several advantages of implementing the variable delay element as a complementary four-transistor stack. First, the pseudodifferential control of the delay value provides a seamless interface with the output of a fully differential loop filter circuit so that common-mode noise in that path is rejected. Second, the topology provides reasonably good linearity in the voltage-to-frequency tuning characteristic of the VCO with a compact and low-power implementation and allows a very large frequency tuning range for the VCO needed to achieve a high range of quantization levels. Third, full-swing CMOS logic levels in the delay element are directly compatible with the standard cell regenerative latches used for the phase register. Finally, the structure supports a high clock rate by achieving a small minimum delay of 35–40 ps in the 0.13 μm CMOS process, which is comparable to a loaded inverted delay in that process. In the prototype, the choice of $N = 31$ elements and $F_{\text{clk}} = 950$ MHz requires a *nominal* delay of 70 ps and, therefore, a *minimum* delay of around 35 ps.

To account for process variation in the center frequency of the oscillator, four gain settings control the level of current drive in the delay cell. As shown in Fig. 10, the 2 bits of tuning can account for approximately $\pm 20\%$ of center frequency variation and are hand-adjusted in this prototype. This constitutes a relatively coarse adjustment of the frequency offset of the VCO tuning characteristic, which is acceptable since any remaining offset simply translates into a differential offset voltage at the input of the VCO tuning port. Of course, in the case of a severe offset, linearity performance will suffer and, ultimately, the open-loop gain of the ADC will significantly drop if frequency saturation occurs in the VCO. Note that the impact of power supply and thermal variations on the oscillator center frequency are mitigated by the feedback having large gain at low frequency, as will be seen in Section VI.

Finally, since excess delay introduced by the quantizer degrades the phase margin of the ADC structure, it is worthwhile

to estimate its value in the proposed VCO-based quantizer structure. To do so, note that V_{tune} is integrated over the previous sampling period which can be seen as a 1/2 clock delay, and the DAC_1 pulse logic begins a half period after the quantizer positive sampling edge. Additionally, there is an estimate of 1/4 clock delay for generating the return-to-zero (RZ) DAC pulses. The combination of these effects leads to an excess loop delay of approximately 1.25 clock periods.

B. DAC

An RZ topology was chosen for the primary DAC in the prototype ADC (i.e., DAC_1 in Fig. 8) in order to minimize the impact of inter-symbol interference at the high sample frequency of 950 MHz and to provide additional compensation of excess loop delay introduced by the VCO-based quantizer. The penalties for choosing an RZ topology are larger current variation at the output summing node, increased sensitivity to clock jitter, and increased power [9]. As mentioned earlier, the issue of current variation was addressed through the use of passive filtering in the prototype. The issue of clock jitter, which strongly impacts the SNR of any high-speed continuous-time $\Sigma\Delta$ ADC structure, was addressed by using a low noise, off-chip clocking source. The issue of power consumption was partially mitigated through circuit design efforts, the details of which are described below.

The schematic for the primary RZ DAC element core is shown in Fig. 11(a), and the overall DAC structure is comprised of 31 unit elements each connected bit-wise to the VCO-quantizer outputs. Degenerated transistors with moderate channel lengths (and accompanying cascode devices) are used on both the top and bottom current sources to minimize thermal and 1/f noise. The output common-mode range of the DAC is set via the low impedance of the input signals, which have a common-mode voltage of half-supply ($V_{\text{DD}}/2$). Large off-chip capacitors are used for both the nMOS and pMOS bias voltages

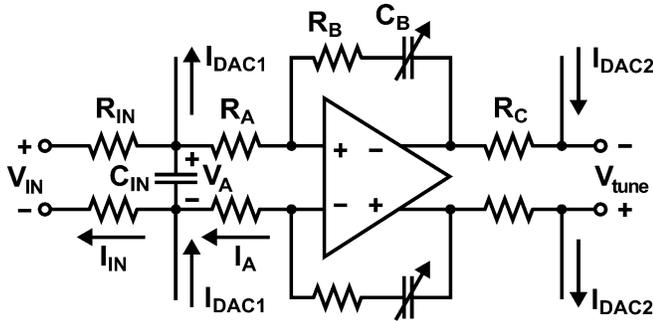


Fig. 12. Schematic of the fully differential ADC loop filter.

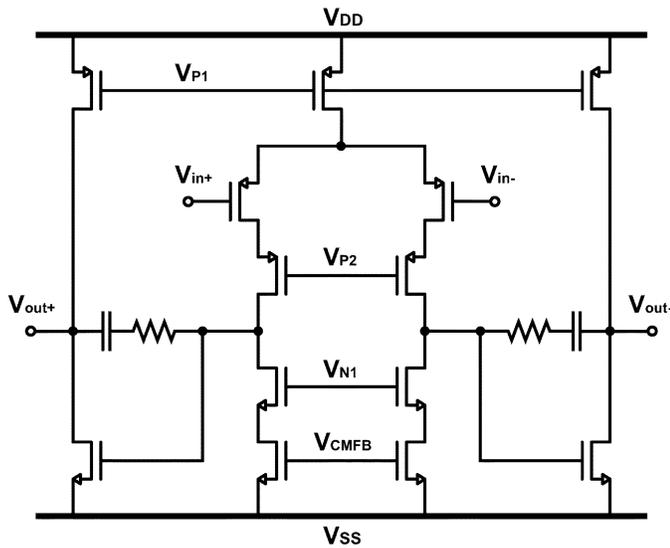


Fig. 13. Opamp schematic.

to reduce the noise coupling from the current reference. The full-scale output current of DAC₁ is ± 9 mA, which corresponds to a full-scale input current of ± 4.5 mA.

As shown in Fig. 11(a), a triple-source configuration steers the current bias to either the positive or negative summing node during the active pulse and to a relatively low impedance node set at $V_{DD}/2$ during the RZ time. This configuration allows the current sources to share current during the RZ time and therefore saves 25% of the current compared with alternative topologies. However, there is still 50% more bias current used in this design than would be for a nonreturn-to-zero (NRZ) implementation.

The RZ DAC switching waveforms are at full-level CMOS logic levels, so the switching transistors see a large overdrive. The on pulse control is output from NAND gates which retimes the data with the negative clock state. Careful attention to balancing the differential signals helps to keep source bounce low during switching events. Again, the power required in generating the switching waveforms for the RZ implementation is significantly higher than for an NRZ DAC, especially considering the 950 MHz sampling rate.

In contrast to the RZ approach used for the primary DAC, the minor loop DAC (which corresponds to DAC₂ in Fig. 8) is implemented as an NRZ structure due to its less stringent performance requirements. The clocking of this DAC is done

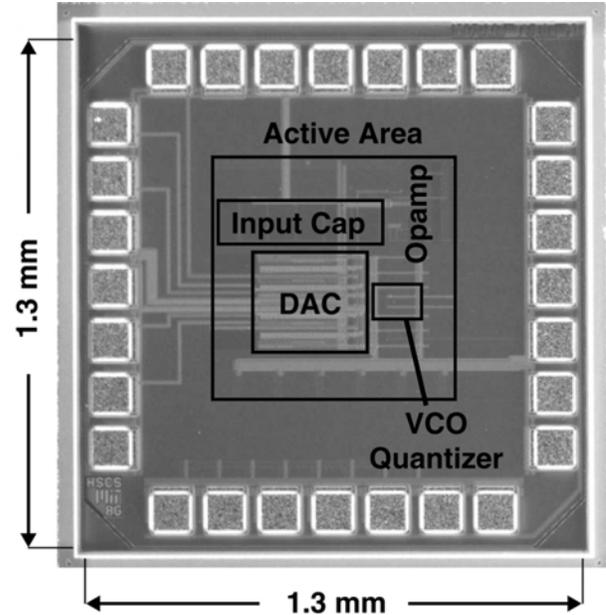


Fig. 14. Microphotograph of the VCO-based ADC.

 TABLE I
 SUMMARY OF VCO-BASED ADC MEASURED PERFORMANCE

Specification	Value
Sampling Frequency	900-1000 MHz
Input Bandwidth	10 / 20 MHz
Peak SNR	86 / 75 dB
Peak SNDR	72 / 67 dB
Analog Power	20mW (1.2V)
Digital Power	20mW (1.2V)
Peak Efficiency	0.5pJ/step
Active Area	640 μ m \times 660 μ m
Total Area	1.3mm \times 1.3mm
Technology	0.13 μ m IBM CMOS

without retiming since the sensitivity to clock jitter and inter-symbol interference (ISI) is suppressed by the forward integration path. The 31-elements of this second DAC are scrambled with the barrel-shift DEM due to the bit-wise connection to the VCO-based quantizer, though the issue of DAC mismatch is not as important for this DAC as the primary one. The full-scale current of DAC₂ is nominally ± 64 μ A and can be adjusted over a wide range through an off-chip bias current such that peaking is properly controlled in the NTF of the ADC. With the minor loop disabled by removing the DAC current bias, the ADC was found to still be marginally stable.

C. Loop Filter

The fully differential loop filter schematic, which uses only a single opamp, is shown in Fig. 12. As mentioned earlier, the loop filter includes a front-end passive filter composed of elements R_{IN} , R_A , and C_{IN} in order to absorb the large current deviations of DAC₁ and provide a very linear ADC front-end. Closer examination of the front-end passive filter reveals that voltage V_A is actually a virtual ground when placed in $\Sigma\Delta$ feedback, so the ADC input current I_{IN} is defined primarily by resistor R_{IN} . The capacitor C_{IN} then filters the error signal $I_{IN} - I_{DAC1}$ before I_A is integrated onto capacitor C_B , whose value can be

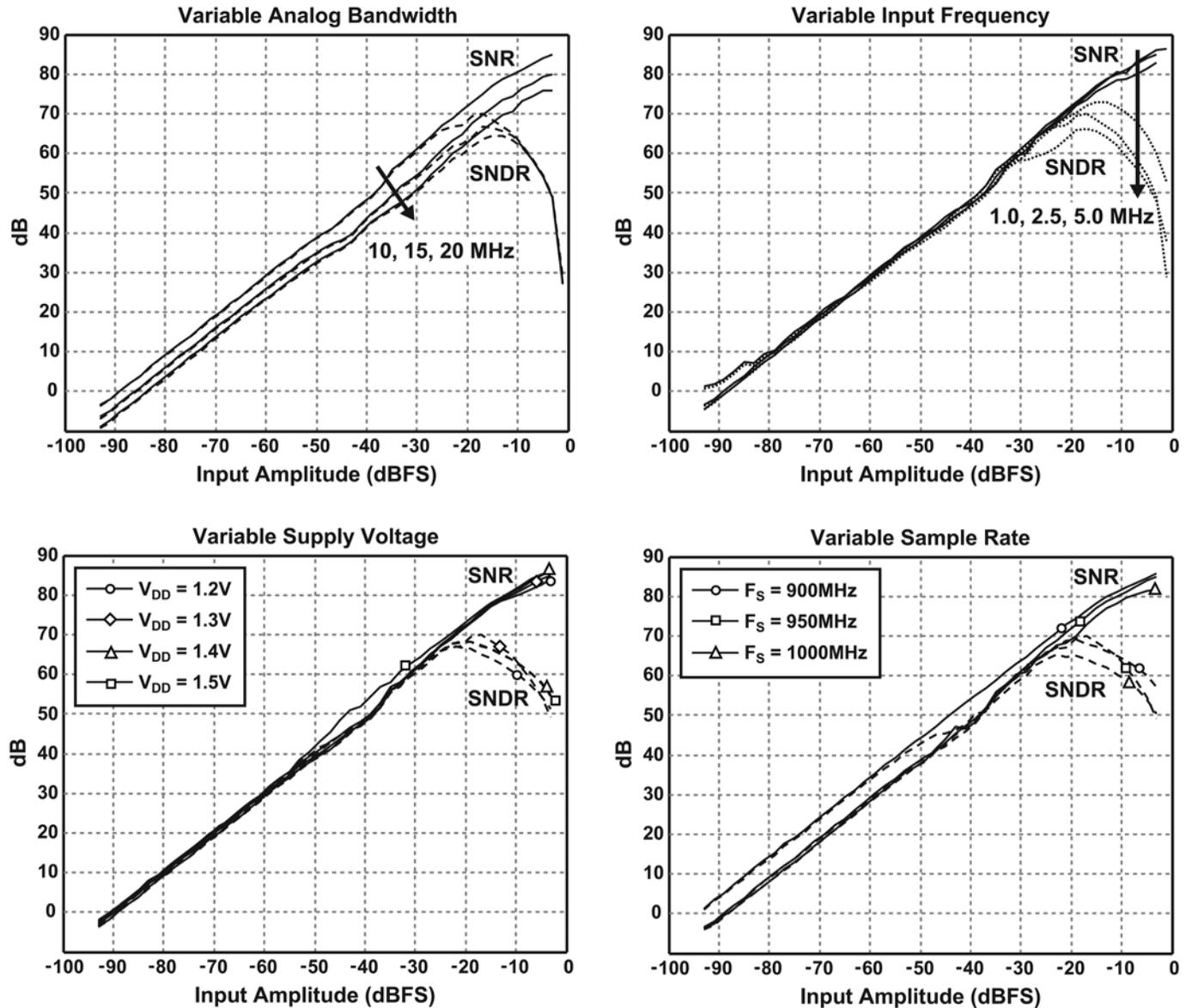


Fig. 15. SNR/SNDR versus input amplitude.

adjusted by $\pm 25\%$ with an on-chip binary capacitor array. Adjustment of C_B leads to a gain change in the active integrator, which allows for better accommodation of K_v variations in the VCO-based quantizer. Of course, changes in C_B will also lead to variation in the value of the open-loop zero formed by C_B and R_B .

The loop-filter opamp is implemented with the two-stage Miller-compensated topology shown in Fig. 13. Since the ADC input is assumed to have a constant common-mode voltage at its input, the first opamp stage can be cascoded even with low supply voltage. Interestingly, because the VCO-based quantizer offers relatively high SNR performance on its own, a large dc open-loop gain is not required for the proposed ADC topology. As such, the gain is designed to be over 50 dB with a gain-bandwidth product in the range of 2–3 GHz. Note that the output common-mode voltage also controls the input common mode of the VCO and is set according to a common-mode

feedback circuit that consists of two large polysilicon resistors, a single-stage amplifier, and an off-chip reference voltage [10].

As mentioned earlier, minor loop feedback is used to compensate for excess loop delay from the quantizer and DAC_1 in order to allow a more aggressive NTF. To avoid the use of another amplifier for a summation operation, current DAC_2 is directed through resistor R_C such that the resulting voltage is added to the output of the opamp. Although the opamp output resistance is nonzero, it is much less than R_C in the frequencies of interest and does not need to be well controlled since the gain and precision of this minor loop is not critical to ADC performance. The value of R_C is chosen to keep the parasitic pole, which is formed by R_C and the input capacitance of the quantizer, from affecting the loop dynamics. The full-scale current of DAC_2 is then set based on the value of R_C and considerations of the NTF. In addition to providing analog summation without an amplifier, another benefit to this topology is that the stability

concerns of the operational amplifier are isolated from the input capacitance of the VCO-based quantizer.

VI. MEASURED RESULTS

A prototype of the ADC structure shown in Fig. 8 was implemented in a $0.13\ \mu\text{m}$ CMOS process. A microphotograph of the fabricated chip is shown in Fig. 14. The active silicon area of the ADC is $640\ \mu\text{m} \times 660\ \mu\text{m}$, including power supply decoupling capacitors and guard ring. Area for the 5-bit VCO-quantizer core is $120\ \mu\text{m} \times 86\ \mu\text{m}$, and the total chip area including 28 pads is $1.3\ \text{mm} \times 1.3\ \text{mm}$. A summary of the ADC performance is found in Table I, where the figure of merit is $\text{Power}/(2 \cdot \text{Bandwidth} \cdot 2^{\text{ENOB}})$.

The power consumption of the ADC is 40 mW, which is evenly split between the 1.2 V analog and digital supplies such that each draw roughly 16–17 mA. Although there is no direct way to measure the subsystem current, bias currents indicate that the primary DAC consumes 9 mA, and the operational amplifier consumes 8 mA. For the digital supply, the pulse-waveform generation circuits for the RZ DAC require about 8 mA, the VCO-quantizer requires 5 mA, and the thermometer-to-binary summation circuits take the remaining 3 mA.

The SNR and SNDR versus input amplitude curves across a number of operating conditions are shown in Fig. 15. If not otherwise specified, the input frequency is 2.5 MHz, the analog bandwidth is 10 MHz, and the sample rate is 950 MHz. At a 10 MHz input bandwidth, the ADC achieves at least 81 dB SNR and 65 dB SNDR across all input frequencies, a power supply of 1.2–1.5 V, and a sampling frequency of 900–1000 MHz. While a peak SNR of 14 bits at 10 MHz is achieved very efficiently with only 40 mW of total power consumption, the ADC distortion performance is limited by the VCO-quantizer nonlinearity to 10.5–12 bits, depending on the specific test configuration.

The decline of SNDR with increasing signal frequency in Fig. 15 is a consequence of the reduced gain of the loop filter at higher frequencies, which leads to reduced suppression of the VCO nonlinearity. The degradation of SNDR by such nonlinearity was about 5 dB higher than predicted by simulation, which is likely due to the modeling accuracy of the VCO tuning characteristic, which can be affected by layout in addition to process and temperature variations. It may be possible to improve the SNDR somewhat with more attention given to modeling these issues, although this would not fundamentally change its frequency dependence.

It was observed that low input signal levels into the proposed ADC led to small limit cycles which were seen in the 10–100 kHz frequency range. These limit cycles are an artifact of the barrel-shift algorithm used for DEM on the DACs, which is why some demanding applications avoid the use of the barrel-shift algorithm in favor of other DEM strategies [11]. These small limit cycles can reduce the SNR by a few decibels when the input signal falls below about $-35\ \text{dBFS}$, as seen in the SNR versus amplitude curves. As would be expected, the actual frequency of the limit cycle depends somewhat on the input dc level.

A fast Fourier transform (FFT) of the ADC output with an 1.045 MHz input signal at $-15\ \text{dBFS}$ is shown in Fig. 16. The third-order noise shaping is visible from 10–50 MHz, and the

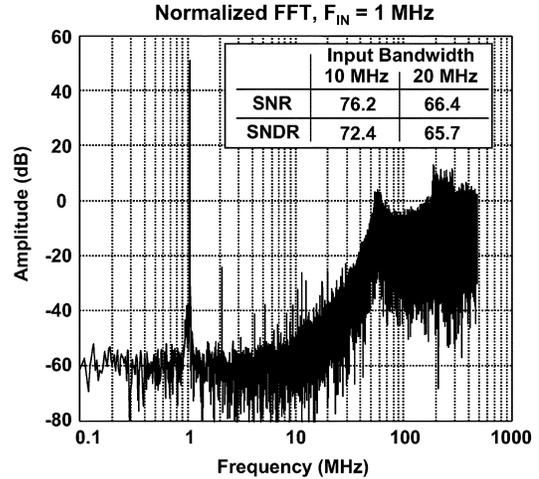


Fig. 16. 190, 190 point Hanning FFT normalized to an LSB.

TABLE II
COMPARISON WITH PUBLISHED HIGH-SPEED CT ADCS

Ref.	F_s (MHz)	BW (MHz)	SNR (dB)	SNDR (dB)	Power (mW)
[12]	276	23	70	69	43
[13]	340	20	71	69	56
[14]	400	12	64	61	70
[15]	640	10	72	66	7.5
[16]	640	20	76	74	20
[17]	1000	8	63	63	10
This work	950	10	86	72	40

quantization noise peaks around 60 MHz. A small noise skirt centered around 1 MHz was found to be from the bandpass filter used in testing. The high-frequency quantization noise feature occurring in the 200–300 MHz range is believed to be a small limit cycle at $F_s/4$ caused by the mismatch between rising and falling edges of the VCO-quantizer, but this has not been experimentally verified. Fortunately, this artifact does not affect the functional operation of the ADC as its stability was seen to be robust across a wide variety of operating conditions.

Finally, Table II compares this work with other reported CT $\Sigma\Delta$ CMOS ADC structures operating at a sampling rate over 250 MHz and with an analog bandwidth of more than 5 MHz. The high SNR of 86 dB achieved in this work points to the strength of the VCO-based quantizer architecture, which provides efficient reduction of quantization noise through its high-speed operation. The SNDR performance and power consumption are in line with other realizations.

VII. CONCLUSION

A very high-speed, low-power CT $\Sigma\Delta$ ADC using a 5-bit VCO-based quantizer that provides inherent DEM matching is implemented in $0.13\ \mu\text{m}$ CMOS. The power- and size-efficient VCO-based quantizer operating at 950 MHz has very low quantization noise, which allows the ADC to achieve 86 dB SNR in 10 MHz bandwidth while consuming 33 mA from a 1.2 V supply. The distortion of the VCO-based quantizer is suppressed by gain from the loop filter, but remains the dominant nonlinearity that limits the peak SNDR performance of the ADC to 72 dB. Prospects for improved performance using the VCO-

quantizer in advanced CMOS processes are good, especially if new techniques can be found to further mitigate the quantizer nonlinearity. Therefore, improving the VCO nonlinearity remains an active area of research, with possible solutions coming from not only better components, but also from investigating ADC topologies that have better nonlinearity suppression.

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